What is claimed is:

1. A phase-change memory element, comprising:

a first electrode used as a heating layer;

a second electrode whose side surface faces a side surface of the first electrode in side direction; and

a memory layer located between the side surfaces of the first electrode and the second electrode and is made of a phase-change material contacting at least the side surface of the first electrode.

2. The phase-change memory element of claim 1, wherein the first electrode and the second electrode are formed of same material.

3. The phase-change memory element of claim 1, wherein the first electrode is made of one selected from the group consisting of titanium aluminum nitride, titanium silicon nitride, and titanium carbon nitride.

4. The phase-change memory element of claim 2, wherein the first electrode and the second electrode have the same thickness and have the same height.

5. The phase-change memory element of claim 1, wherein the first electrode has narrow width portion protruding toward the side surface of the second electrode located opposite to the first electrode and contacting the memory layer.

6. The phase-change memory element of claim 1, wherein chalcogenide alloy is used as the phase-change material.

7. The phase-change memory element of claim 1, wherein the memory layer is formed in a ring shape with its two opposite surfaces contact the side surfaces of the first electrode and the second electrode, respectively.

8. The phase-change memory element of claim 1, further comprising:

a first interconnection contact connecting the first electrode to a semiconductor substrate electrically; and

a second interconnection contact connecting the second electrode to an upper electric line electrically.

9. The phase-change memory element of claim 8, further comprising:

a first electrode pad being between the first electrode and the first interconnecting contact and having a thicker thickness than the first electrode; and

a second electrode pad having the same height and thickness as the first electrode pad under the second electrode.

10. A method of manufacturing a phase-change element, comprising:

forming an electrode layer pattern on a first insulating layer;

forming a second insulating layer covering the electrode layer pattern;

forming a contact hole, through the second insulating layer and the electrode layer pattern that dividing the electrode layer pattern into a first electrode, which is used as a heating layer, and a second electrode layer, which sidely is opposite to the first electrode; and

forming a memory layer with a phase-change material contacting the side surfaces of the first electrode and the second electrode, which are exposed by the contact hole, in the contact hole.

11. The method of claim 10, wherein the forming the electrode layer pattern comprises:

forming the electrode layer pattern on the first insulating layer; and

patterning the electrode layer so that a portion of the electrode layer pattern between the first electrode and the second electrode to the first electrode layer side has narrower width than that of the second electrode; and

the contact hole is formed to cross secting the narrowed width portion and allows the cross secting surface of the narrow width portion to contact with the memory layer.

12. The method of claim 11, further comprising:

forming a first electrode pad and a second electrode pad, respectively aligned to the first electrode and the second electrode, on the first insulating layer prior to the formation of the electrode layer.

13. The method of claim 12, wherein the forming the first electrode pad and the second electrode pad comprises:

forming an electrode pad on the first insulating layer; and

patterning the electrode layer to form the first electrode pad and the second electrode pad.

14. The method of claim 11, further comprising:

forming an interconnection contact, which electrically connects a semiconductor substrate thereunder, and the first electrode through the first insulating layer prior to the formation of the electrode layer.

15. The method of claim 10, wherein the forming the memory layer comprises:

forming the memory layer at least contacting the side wall of the contact hole; and

patterning the memory layer by a CMP process to expose the upper surface of the second insulating layer.

16. The method of claim 10, the forming the memory layer comprises:

forming the memory layer at least contacting the side wall of the contact hole and following the profile of the above contact hole; and

patterning the memory layer to have a ring shape on the wall of the contact hole that exposes the bottom of the contact hole.

17. The method of claim 13, the forming the memory layer comprises:

patterning the memory layer by etching back the memory layer.

18. The method of claim 10, further comprising:,

forming a third insulating layer on the second insulating layer; and

forming an upper electric line on the third insulating layer to electrically connect to the second electrode after forming the memory layer.